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DESIGN AND IMPLEMENTATION OF AN RF BALANCED AMPLIFIER FOR WIRELESS COMMUNICATION SYSTEMS

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ABSTRACT

This paper involves a design and implementation of a radio-frequency (RF) balanced amplifier for modern wireless communication systems. The proposed circuit consists of two identical microwave GaAs pseudomorphic high electron mobility transistor (pHEMT) amplifiers connected together using 3-dB hybrid couplers. The input and output matching circuits for each transistor are designed using microstrip lines to ensure low input/output voltage standing wave ratio (VSWR) and stable operation. The amplifier circuit is initially designed and simulated with the aid of the Keysight's ADS software to operate in the mobile communication band from 850 to 950 MHz. The circuit has then been implemented and tested practically in the laboratory. The measured performance results show a power gain of 15 dB at the desired frequency band and a 1-dB gain compression point output RF power of +19 dBm at the center frequency of the band.

KEYWORD:- RF Amplifiers, Balanced Amplifier, pHEMT, Microstrip Matching Networks, Branch Line Couplers.

1 .INTRODUCTION

RF/Microwave amplifiers are key elements in modern solid-state wireless transmitters and receivers. Important parameters of microwave amplifiers include high power gain, low noise figure, low input/output return loss, high stability, good linearity, and wide bandwidth. However, not all these parameters can be achieved simultaneously using a single-ended RF amplifier, and therefore designers tend to fulfill some of the performance characteristics at the expense of other parameters. For example, it is difficult to achieve a low noise figure and low input return loss at the same time. Similarly, the insurance of stable operation may be achieved with some loss in power gain. The balanced amplifier is a well-known configuration consisting of two single-ended amplifier units that are connected in parallel via two directional couplers. It can be used to maintain low input/output VSWR regardless of the return losses for the individual stages [1]. Therefore, the balanced configuration can be used to improve the RF performance of the amplifier but with some increase in circuit complexity and size.

Several research works have been conducted to investigate the operation of microwave-balanced amplifiers. A design and simulation of a broadband balanced amplifier operating from 0.8 to 1.7 GHz was carried out by means of low-cost SiGe hetero-junction bipolar transistors (HBTs) and Wilkinson couplers [2]. It was shown that a low noise figure and a reduced input reflection coefficient can be achieved theoretically over a considerable band of frequencies. Similarly, an ISM-band balanced amplifier has been designed and simulated using the Wilkinson power divider/combiner and GaAs MESFETs with an output RF power of 16 dBm at 2.45 GHz [3]. However, the use of Wilkinson couplers implies the insertion of additional delay lines at the individual amplifiers to produce the necessary phase shifts which increases the complexity of the circuit. A modified balanced amplifier technique is proposed by injecting the reflected input power from the isolated port of the input coupler into an extra amplifier and connecting its output to the isolated port of the output coupler [4]. It was verified that this method can increase the power gain, output RF power, and power-added efficiency of the conventional balanced amplifier at the expense of increased complexity. The linearity of the balanced amplifier has been improved through the use of digital predistortion technique for an amplifier operating in the C-band [5]. A low-noise balanced amplifier was implemented using GaAs HEMT microwave

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monolithic integrated circuits (MMICs) [6]. Superior performance characteristics were obtained through the balanced configuration like low noise figure, low input reflection coefficient, high gain, good linearity, and high stability. Another Ka-band high gain and low noise balanced amplifier was synthesized using the pseudomorphic high-electron-mobility transistor (pHEMT) on a chip to operate within the wideband frequency range from 30 to 36 GHz [7]. An efficient and linear power amplifier can also be designed and simulated based on the balanced configuration through the use of Lateral MOSFET transistors biased in the class-AB mode for LTE band applications [8]. A wideband class-AB power amplifier using the balanced topology was simulated to operate from 400 MHz to 1.4 GHz with good gain flatness and linearity in addition to low input/output return loss [9].

The size of the balanced amplifier can be reduced by using compact couplers instead of the conventional branch-line couplers. A method for implementing the coupler using a U-shaped transmission line has been presented and a miniaturized balanced power amplifier was designed using these new types of couplers [10]. The resulting amplifier performance shows lower input and output VSWR and higher saturated output power over the single-ended amplifier. A balanced class-F power amplifier using novel compact couplers is also presented [11]. The couplers are synthesized using rhombus-shaped resonators and have the capability of harmonic suppression, thereby improving the linearity of the resulting balanced amplifier.

A mathematical analysis for the VSWR withstand capability of the balanced power amplifier is conducted to show the impact of the load mismatch on the individual transistors of the balanced amplifier [12]. The balanced amplifier configuration has also been used to improve the power-added efficiency of a power amplifier operating in the S-band region using Lange-couplers and GaAs pHEMT chip devices [13].

Recently, a novel efficiency enhancement technique for power amplifiers based on the balanced amplifier topology has been developed [14-16]. This technique, known as the load-modulated balanced amplifier (LMBA), uses an additional control signal generated from an auxiliary amplifier and injected into the isolation port of the output 90^o coupler so as to modulate (change) the load impedance seen by the individual transistors of the balanced amplifier.

In this article, a balanced amplifier has been designed and implemented using discrete GaAs pHEMT RF transistors and 90^o hybrid couplers to operate in the communication band 850-950 MHz. The balanced configuration has been selected to guarantee low input/output reflection loss, facilitate the cascading capability of the amplifier circuit, and to increase the output linear power. The GaAs pHEMT active devices have been chosen since they have low internal paracitic capacitances and high electron mobility, leading to superior RF performance at high frequencies. Measured performance results show improved linearity and enhanced output RF power.

2 .THE BALANCED AMPLIFIER CONFIGURATION

The balanced amplifier consists of two single-ended amplifiers connected in parallel via two hybrid couplers as shown in Fig. 1 [17]. The input and output matching networks of each amplifier are designed to achieve optimum power gain, noise figure, and output RF power. The input branch-line coupler introduces a phase shift of 90^o between the signals provided to the two amplifiers, while the output coupler equalizes the phase difference.

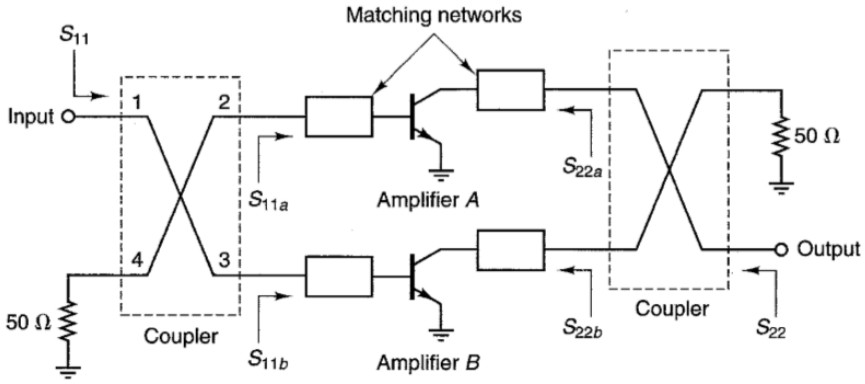


Fig. (1):- Topology of the balanced amplifier [17].

The driving signal is equally split by the input coupler (power divider) into two waves at the input networks of the amplifiers and then recombined by the output coupler (power combiner) at the output of the circuit, while the power at port 4 is ideally equal to zero. A schematic diagram for the branch line coupler is presented in Fig. 2. It consists of two horizontal λ/4 parallel transmission lines with a characteristic impedance of $Z_0/\sqrt{2}$ and two shunt λ/4 lines with a characteristic impedance of Z_0 [18].

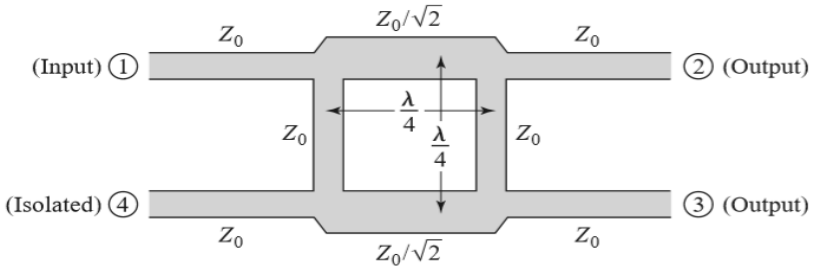


Fig. (2):- The branch-line 3-dB coupler [18].

With an incident wave a_1 at port 1, the received wave b_2 at port 2 contributes a phase shift of 90° due to the λ/4 transmission line of the coupler. On the othe hand, the signal at port 3 travels across two λ/4 transmission lines and hence the received wave b_3 at port 3 exhibits a phase shift of 180°. With a matched impedance of 50 Ω at ports 1 and 4, the reflected waves $b_1 = b_4 = 0$.

For identical amplifier units, the overall input and output reflection coefficients of the balanced amplifier are ideally equal to zero. On the other hand, the power gain of the balanced amplifier is equal to that of amplifiers *A* and *B*. However, the maximum output RF power that can be obtained from the balanced amplifier is twice that of the individual amplifiers [17].

3 .DESIGN OF THE BALANCED AMPLIFIER CIRCUIT

In this section, the design details for a medium-power RF amplifier operating within the frequency band from 850 MHz to 950 MHz are presented. This frequency range includes the American ISM band (902-928 MHz), and the European ISM band (863-870 MHz) [19]. Design objectives are to achieve high power gain, low input/output return loss, high stability, and good linearity.

3.1 Transistor Selection and Characterization

The ATF-34143 GaAs pHEMT microwave transistor was selected to build the amplifier circuit. It is a low-cost depletion-mode device housed in a SOT-343 surface-mounted package. This device offers a low noise figure, high power gain, and can provide an output RF linear power of +20 dBm.

A bias point with V_D = 4 V and I_D = 60 mA was chosen to obtain high power gain. The transfer characteristic of the FET was simulated using Keysight's ADS software and is sketched in Fig. 3. As shown from this figure, for a drain current of 60 mA, the required gate-to-source voltage is approximately equal to -0.44 V. The pinch-off voltage of the pHEMT transistor is

about -0.9 V. This shows the high sensitivity of drain current for a small change in the gate bias voltage.

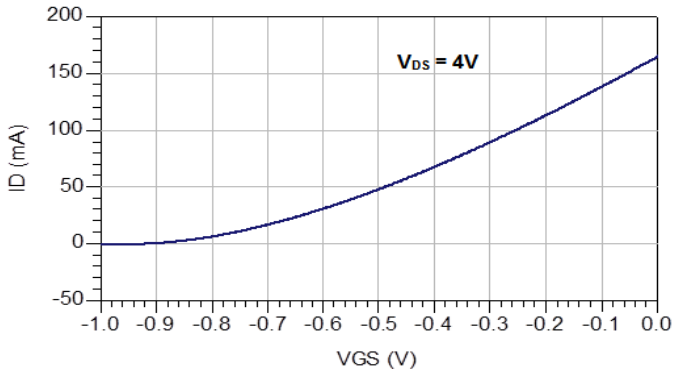
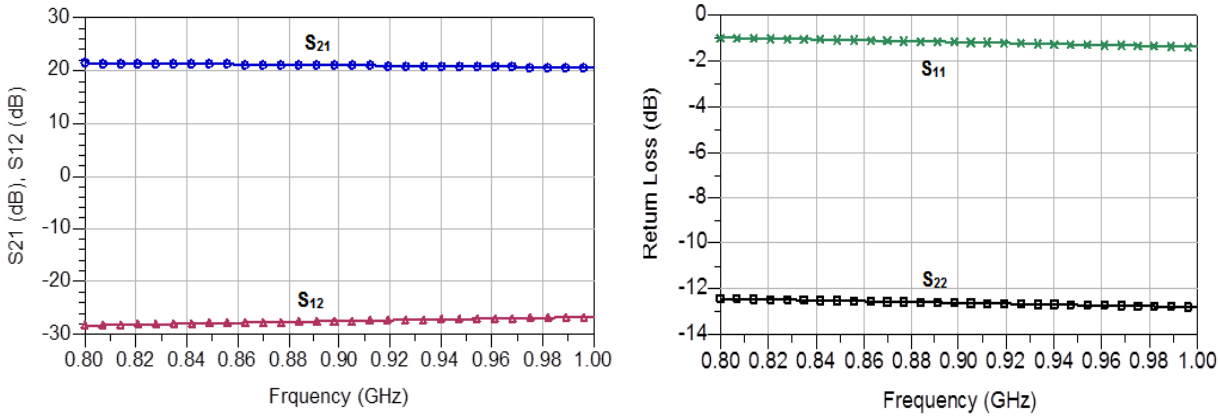


Fig. (3):- Simulated transfer characteristic of the ATF-34143 GaAs pHEMT.

The S-parameters of the transistor at the desired *Q*-point and over a frequency range from 800 MHz to 1 GHz were simulated, as shown in Fig. 4. As it is clear from this figure, the transistor can achieve a power gain of 20 dB without matching. However, the input reflection coefficient was significantly high, which necessitates the need for a matching network. Besides, the simulated stability factor, *K*, is lower than 1 across the same frequency range as shown in Fig. 5, and therefore a stability resistor should be inserted in the amplifier circuit to prevent any tendency towards oscillation.



(*a*) **(*b*)**

Fig. (4):- Simulated S-parameters of the pHEMT transistor. (a) S_{21} and S_{12}, (b) S_{11} and S_{22}.

The value of the stability resistor can be found from the circuit simulation to increase the stability factor above 1. If the stability resistor is placed in the input network of the active device then this will degrade the noise figure. On the other hand, inserting the stability resistor at the output port of the transistor will decrease the power gain and output RF power.

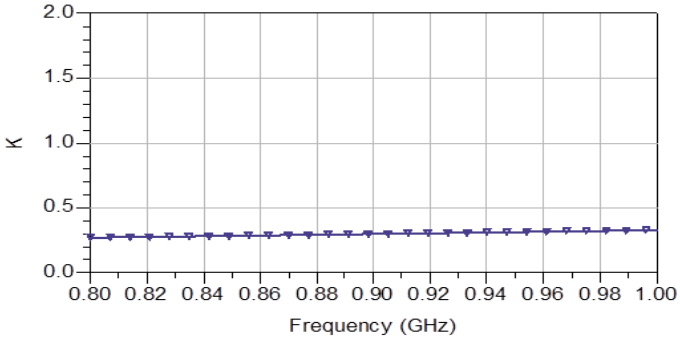


Fig. (5):- Stability Factor versus Frequency.

3.2 Design of the Matching Networks

In order to achieve optimum power gain and input/output VSWR, the matching networks should be synthesized for conjugate matching at the input and output ports of the transistor. To increase the stability factor of the active device, a resistance of 39 Ω was inserted in series with the gate circuit of the FET. The S-parameters of the resistor-FET combination were then extracted by means of the ADS simulator. The simultaneous conjugate match source and load impedances were evaluated at the center frequency of the band, i.e. at 900 MHz, using ADS tools. The optimum source impedance Z_{SM} = 31.838+j74.947 Ω, while the optimum load impedance Z_{LM} = 20.10 + j20.0 Ω at 900 MHz. The graphical design of the input matching network on an Immittance Smith chart is illustrated in Fig. 6, where it consists of a series transmission line and a parallel short-circuited stub. Similarly, the graphical design of the output matching network is presented in Fig. 7 showing a combination of a series transmission line and a shunt open stub.

The ideal transmission line segments are then converted to microstrip lines which can be printed in the form of a PCB board using an FR-4 (epoxy-glass) substrate with a dielectric constant of 4.37, substrate height of 1.52 mm, conductor thickness of 35 µm, and dielectric loss tangent of 0.022. The microstrip line lengths and widths have been tuned for practical purposes. The schematic diagram of the single-ended amplifier circuit is presented in Fig. 8. The gate and drain bias voltages were connected to the transistor via two RF chokes, and bypass capacitors were used to present AC grounds. Two coupling capacitors were utilized to block the DC current from the source and load terminals. The short-circuited stub at the input matching network was connected to the ground using a 100 pF bypass capacitor. Two microstrip T-junctions were used to fill the microstrip discontinuities between the stubs and series lines.

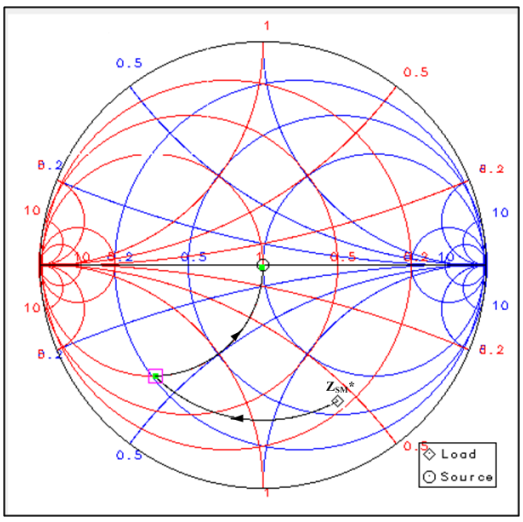


Fig. (6):- Graphical Design of the Amplifier's Input Matching Network.

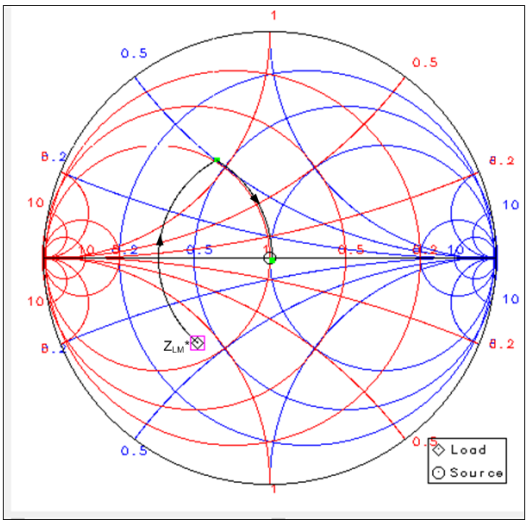


Fig. (7):- Graphical Design of the Amplifier's Output Matching Network.

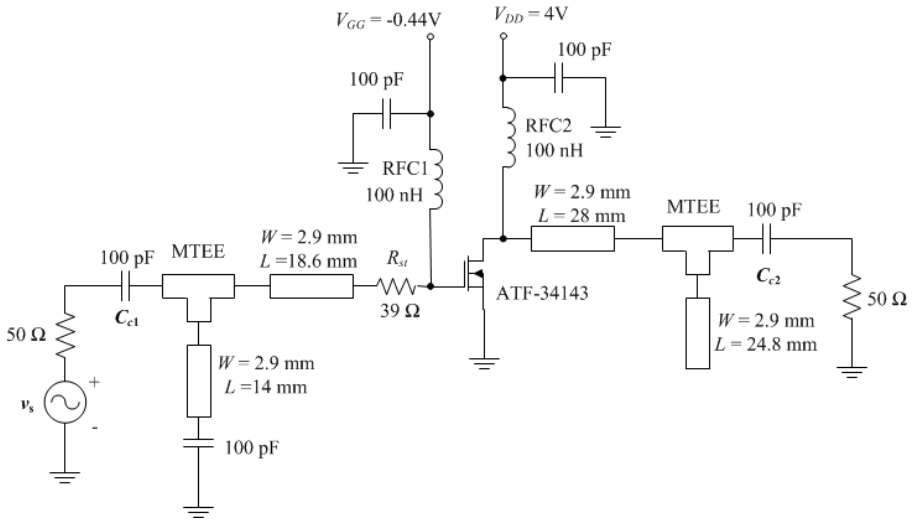


Fig. (8):- Schematic diagram of the designed single-ended amplifier.

The simulated power gain of the single-ended amplifier is displayed in Fig. 9, where it is around 20 dB across the band of interest. On the other hand, Fig. 10 shows the input and output return losses over the same band. The input and output reflection coefficients are both less than -10 dB, confirming the successful effect of the matching networks. Finally, the stability factor, *K*, is sketched in Fig. 11 with a resultant value greater than 1 across the entire frequency band when compared with Fig. 5 due to the effect of the stabilizing resistance.

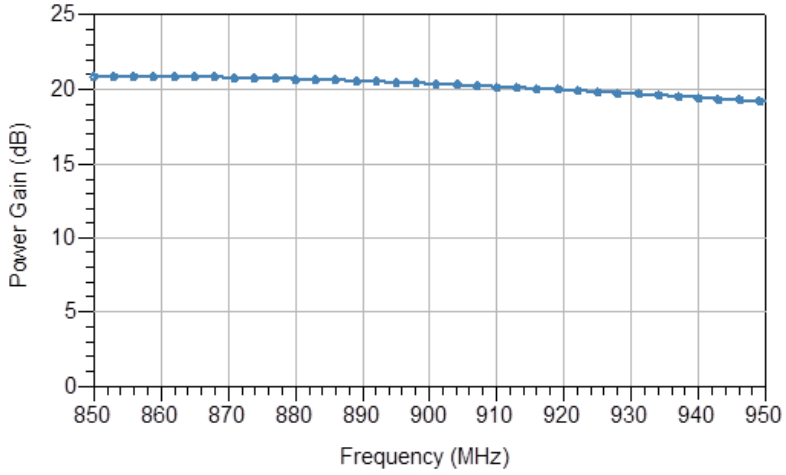


Fig. (9):- The Simulated power gain of the single-ended amplifier versus frequency.

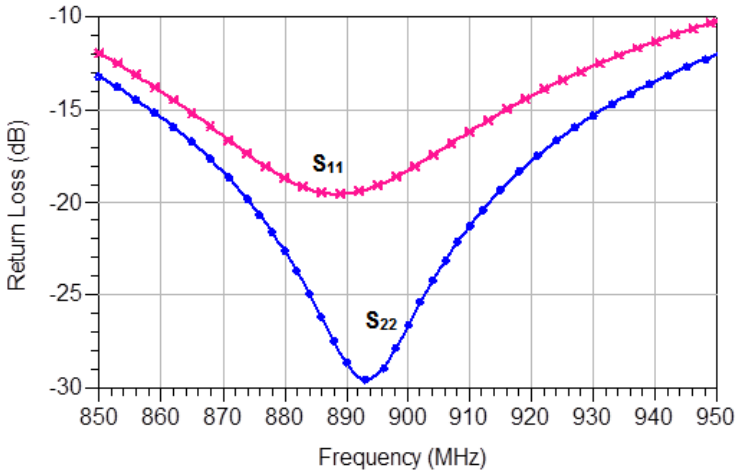


Fig. (10):- Input and output reflection coefficients versus frequency for the single-ended amplifier.

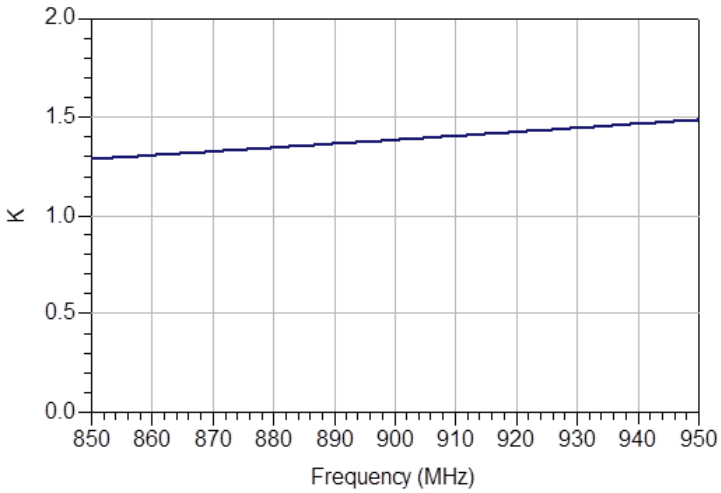


Fig. (11):- Stability factor versus frequency for the single-ended amplifier.

3.3. Design of the Branch-line Couplers

The branch-line coupler presented in Fig. 2 consists of two horizontal parallel transmission lines with a characteristic impedance of 35 Ω and an electric length of 90º in addition to two shunt lines with a characteristic impedance of 50 Ω and an electric length of 90º. These ideal transmission lines are converted to microstrip lines with the appropriate line widths and lengths that are implemented on the FR-4 dielectric substrate. All line lengths are calculated at the center frequency of the band. Fig. 12 depicts the

structure of the branch-line coupler.

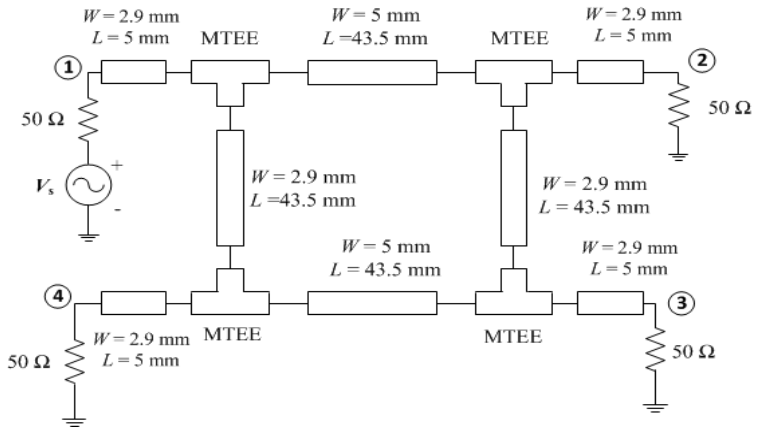


Fig. (12):- Structure of the designed branch-line 3-dB coupler.

It is assumed that the signal is excited from port 1, while port 4 is isolated with a 50 Ω resistor. Ports 2 and 3 are the output ports. The insertion losses S_{21} and S_{31} are displayed in Fig. 13 versus frequency, with a value of around -3.35 dB at the center frequency. The signal power is therefore divided equally between ports 2 and 3. The additional small losses are referred to the dielectric loss of the substrate, microstrip-line discontinuities, and field dispersion. The return loss S_{11} at port 1 is sketched in Fig. 14 with values less than -18 dB across the desired frequency range. The return losses S_{22} and S_{33} at ports 2 and 3 are approximately identical to S_{11}.

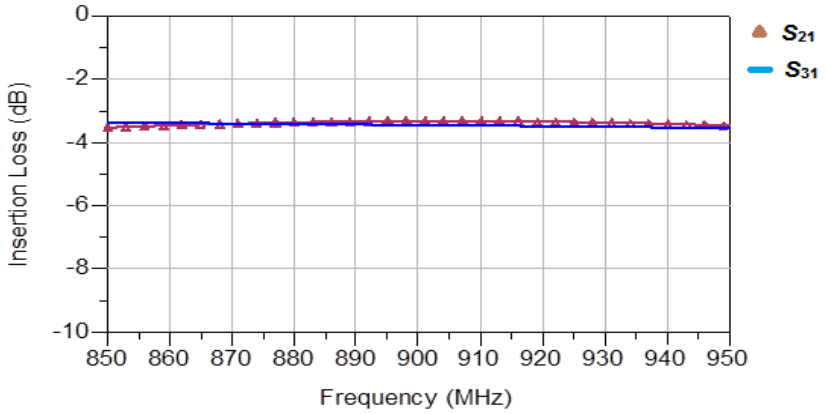


Fig. (13):- The Simulated insertion loss at ports 2 and 3 of the coupler.

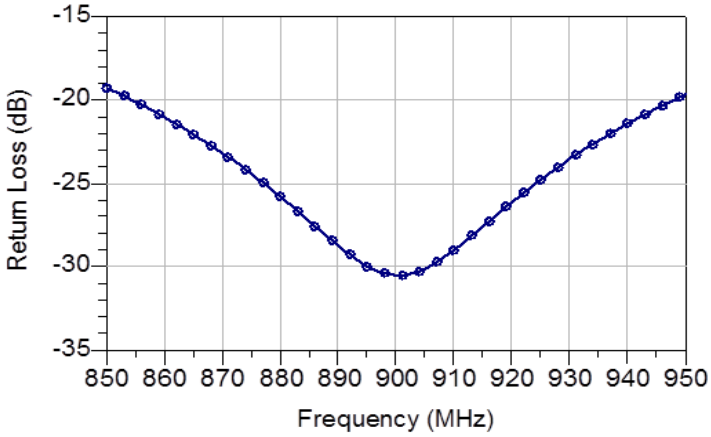


Fig. (14):- Input return-loss of the coupler, S_{11}.

3.4 Design of the Final Amplifier

The final balanced amplifier circuit has then been designed from the combination of the branch-line couplers and two single-ended

amplifiers as illustrated in the block diagram of Fig. 1. The schematic diagram of the RF balanced amplifier is presented in Fig. 15. The dimensions of the microstrip lines were optimized to improve the RF performance of the circuit.

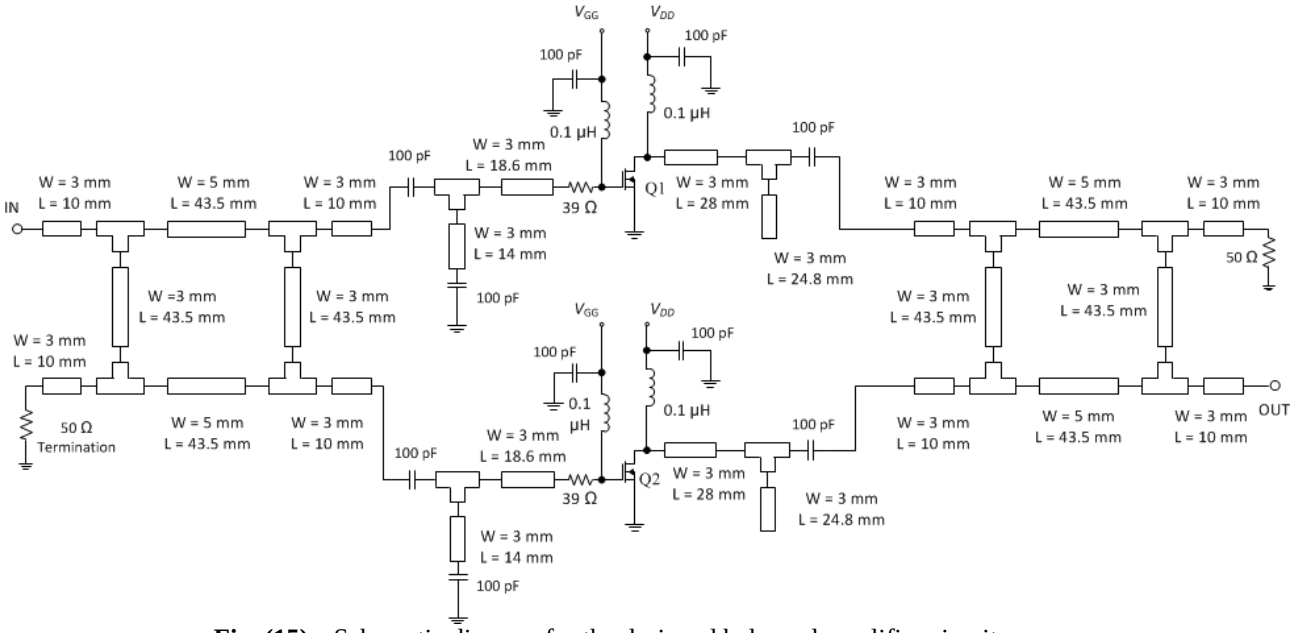


Fig. (15):- Schematic diagram for the designed balanced amplifier circuit.

The optimized power gain of the amplifier circuit is sketched in Fig. 16, showing a gain of 18±0.5 dB across the entire band. The input and output return losses are presented in Fig. 17. It seems that both S_{11} and S_{22} are less than -10 dB over the specified bandwidth. Finally, the stability factor is shown in Fig. 18 and is greater than 1, revealing a stable operation.

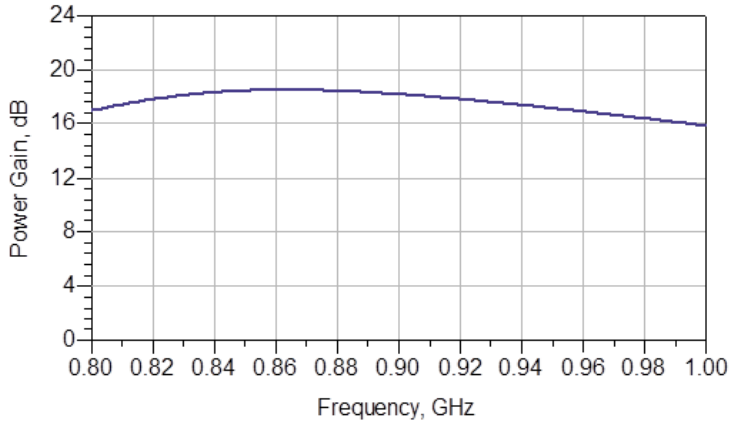


Fig. (16):- Power gain versus frequency for the designed balanced amplifier.

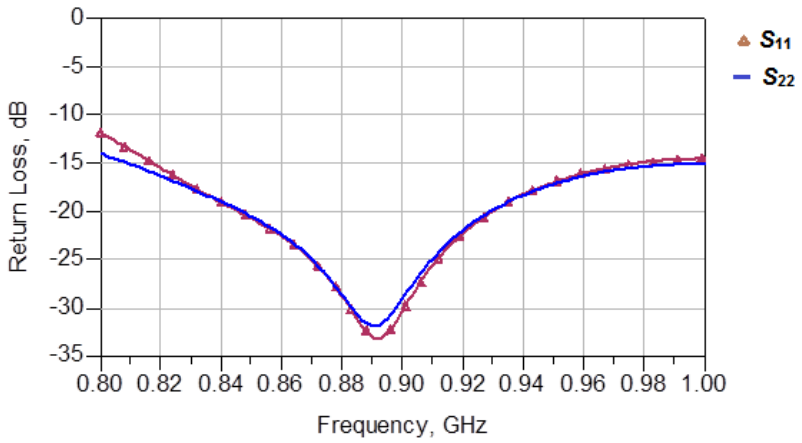


Fig. (17):- Input and output return loss of the optimized amplifier.

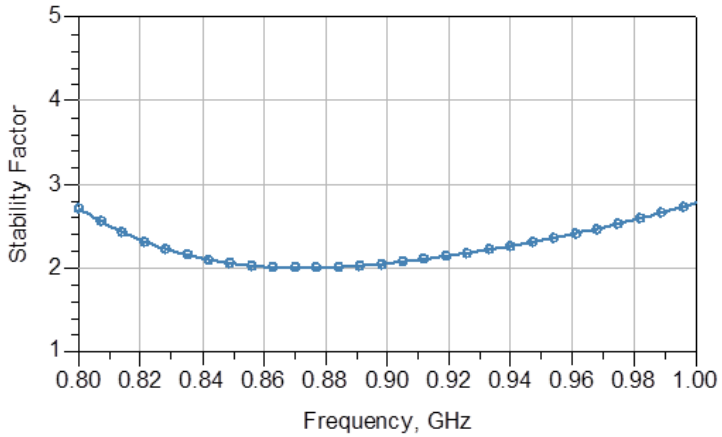


Fig. (18):- Stability factor versus frequency for the optimized amplifier circuit.

3.5.Amplifier Circuit Fabrication and Testing

In order to implement the amplifier circuit practically, a two-sided printed circuit board (PCB) was designed and manufactured. The upper ground tracks were connected to the lower ground side of the board using VIA holes. The components of the amplifier circuit were then soldered on the board. Chip capacitors and resistors were used to minimize the parasitic elements that may degrade the RF performance of the circuit. Axial molded inductors with a value of 0.15 µH were used as RF chokes. The isolated ports were connected to 50 Ω dummy loads. The assembled amplifier circuit is shown in Fig. 19 below.

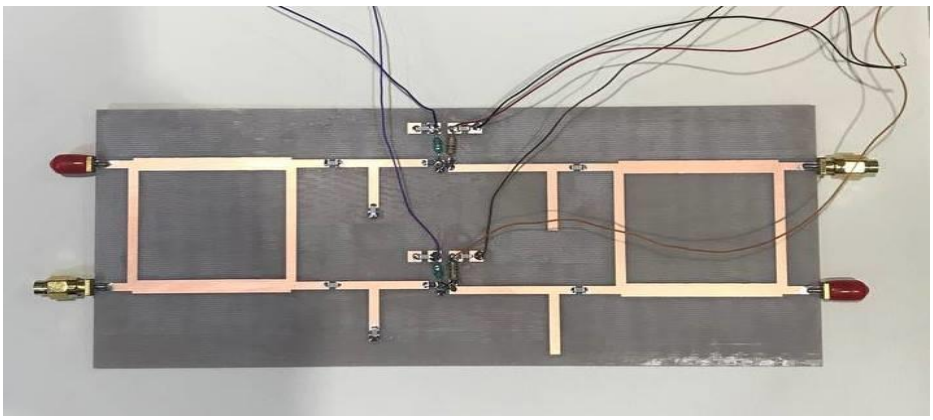


Fig. (19):- A picture showing the assembled RF amplifier.

The amplifier circuit was tested with the aid of an RF signal generator, and a spectrum

analyzer to measure its power gain with frequency. The gate bias voltage was adjusted to set the drain current for each transistor to be 60 mA. It was noticed from the practical measurement that the circuit was initially unstable and produced spurious frequency components due to improper decoupling of the bias circuit. However, this problem was overcome by connecting additional bypass capacitors to suppress the low-frequency oscillations. The proper grounding of the circuit is also very necessary for stable operation. Fig. 20 shows the measurement setup of the amplirfier circuit.

Fig. (20):- Practical test setup of the RF amplifier circuit.

A small signal with a power level of -20 dBm has been applied to the amplifier's input, and the output signal power level is monitored by the spectrum analyzer for different frequencies starting from 850 MHz up to 950 MHz. The output signal spectrum was displayed on the spectrum analyzer PSA-3000 at the center frequency f_o = 900 MHz as shown in Fig. 21.

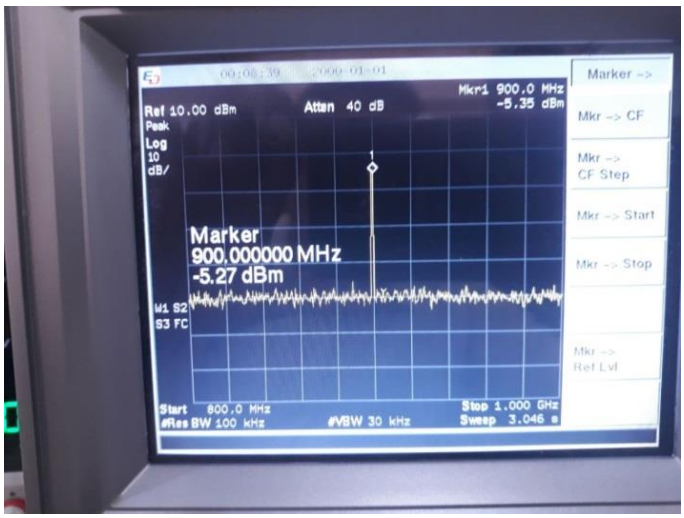


Fig. (21):- Output signal level at 900 MHz for input power of -20 dBm.

The power gain of the circuit has been calculated from the following equation for each frequency:

$$G_p(dB) = P_{out}(dBm) - P_{in}(dBm) + L_c(dB) \qquad (1)$$

where P_{out} is the output power level, P_{in} is the input power level, and L_c represents the cable loss which is approximately 0.25 dB. It is seen that the power gain is about 15.09 dB at 900 MHz.

Fig. 22 shows the measured power gain versus frequency compared with the simulated gain. The practical power gain is approximately 15±0.5 dB across the band of interest. The difference between the simulated and measured

gain is referred to the parasitic components that are added through the implementation process and also to the difference between the actual physical transistor model and the CAD model.

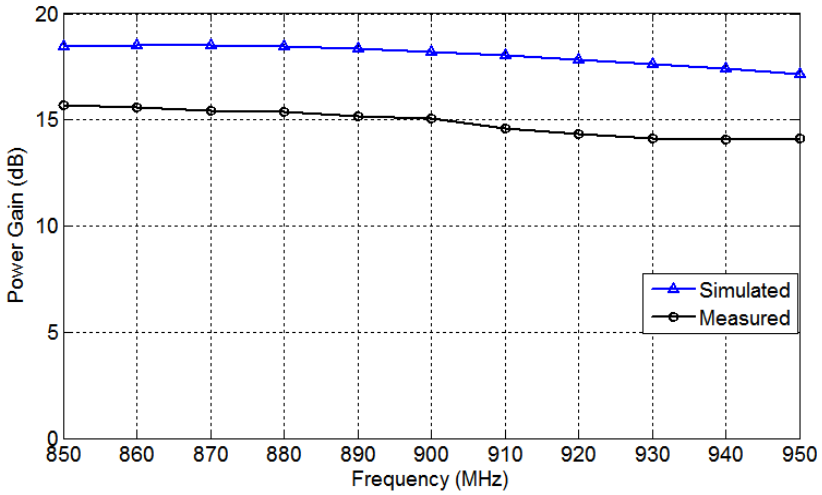


Fig. (22):- Comparison between the simulated and measured power gain of the balanced amplifier circuit.

Fig. 23 presents the output RF power against input drive power at an operating frequency of 900 MHz. It was noted that the 1-dB gain compression point occurs when P_{in} = 7 dBm. The maximum linear output power (P_{1dB}) at this input level is about 19.5 dBm. After this value of input drive power, the power gain starts to compress and the output power begins to saturate slightly due to non-linear operation of the amplifier. However, the characteristic shows the linear operation of the amplifier. Finally, the second harmonic level is shown in Fig. 24 for an input power of +7 dBm at a frequency of 900 MHz. The second harmonic is approximately 42 dBc below the fundamental signal, which means good linearity of the designed amplifier.

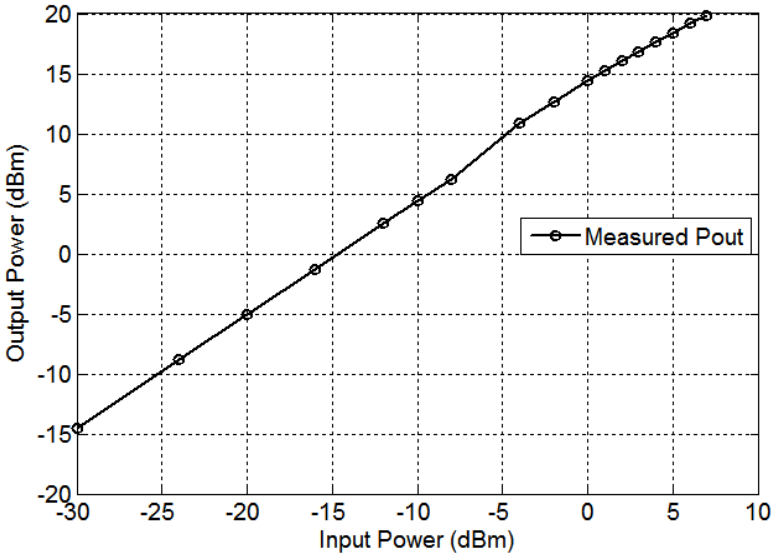


Fig. (23):- Output power versus input power at 900 MHz.

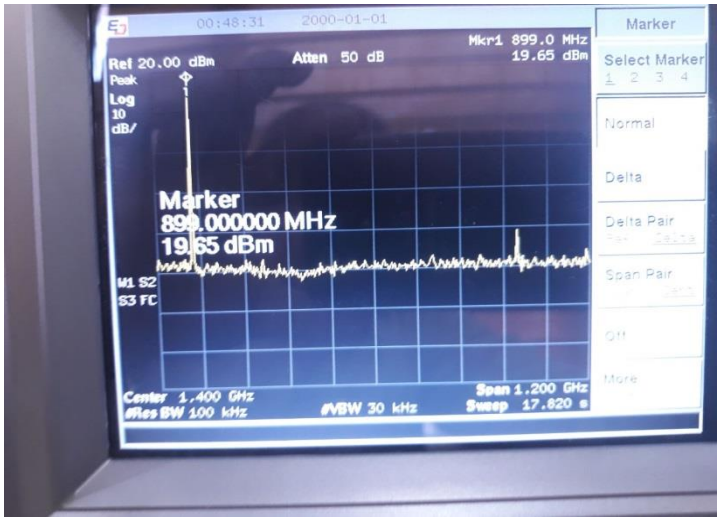


Fig. (24):- The spectrum of the output signal showing the second harmonic component at a fundamental frequency of 900 MHz.

4 . CONCLUSION

A microwave-balanced amplifier circuit has been designed and implemented to operate in the mobile communication frequency band from 850 MHz to 950 MHz. The design procedure involves the use of a powerful microwave CAD program to optimize the initial graphical design of the matching networks and simulate the performance characteristics. The stable operation of the circuit has been guaranteed by the insertion of a stability resistor at the input matching network.

The amplifier circuit was thereafter constructed and tested practically in the laboratory. A typical power gain of 15 dB was obtained at the center of the band, with a maximum linear output power of 19.5 dBm. However, the power gain is somewhat lower than the simulated value by about 2.5 dB. This is referred to the parasitic elements constituted during the fabrication process and soldering. Besides, the design was carried out based on the datasheet transistor *S*-parameters rather than measuring these parameters with a vector network analyzer (VNA). The linearity of the amplifier was tested, showing a 1-dB gain compression output power (P_{1dB}) of +19.5. The second harmonic level was measured to be about 42 dBc below the fundamental signal component at 900 MHz and an input power level of +7 dBm, verifying acceptable linearity. The main advantage of the designed balanced amplifier is increasing the maximum output power by 3 dB over the single-ended amplifier. Besides, the use of couplers at the input and output improves the return loss at both ports. Future work may involve designing other compact couplers to reduce the size of the circuit.

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